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09/920192  
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Class	Subclass	ISSUE CLASSIFICATION



PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E. <i>hlp</i> SCANNED <i>AB4</i> G.A. <i>TM</i>	PATENT DATE
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APPLICATION NO. 09/920192	CONT/PRIOR D	CLASS 029	SUBCLASS 840	ART UNIT 3729	EXAMINER <i>Trinh</i>
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APPLICANTS	Vivek Jairazbhoy Thomas Krautheim Mohan Paruchuri Lakhi Goenka
	TITLE Method for making an electronic circuit assembly

PTO-2040  
12/99

ISSUING CLASSIFICATION									
ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
INTERNATIONAL CLASSIFICATION									

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<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	_____ (Assistant Examiner) _____ (Date)			<b>NOTICE OF ALLOWANCE MAILED</b> _____	
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<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) _____ (Date)			<b>ISSUE BATCH NUMBER</b> _____	
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